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- (56)
- References Cited**

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|-----------|---|---------|----------------|
| 4,307,510 | A | 12/1981 | Sawyer et al. |
| 4,322,253 | A | 3/1982 | Pankove et al. |

(Continued)

- FOREIGN PATENT DOCUMENTS

- | | | |
|----|----------|---------|
| CN | 2550906 | 5/2003 |
| DE | 10017137 | 10/2000 |

(Continued)

- ## OTHER PUBLICATIONS

- Hydrick et al. "Chemical Mechanical Polishing of Epitaxial Germanium on SiO₂-patterned Si(001) Substrates," ECS Transactions. Oct 16, 2008. (oo. 237-248). Hydrick et al., "Chemical Mechanical Polishing of Epitaxial Germanium on SiO₂-patterned Si(001) Substrates," ECS Transactions. Oct. 16, 2008. (oo. 237-248).*

(Continued)

Primary Examiner — Cuong Q Nguyen

- Assistant Examiner — Yosef Gebreyesus

(74) *Attorney, Agent, or Firm* — Slater & Matsil, L.L.P.

- (57)

ABSTRACT

A device includes a crystalline material within an area confined by an insulator. A surface of the crystalline material has a reduced roughness. One example includes obtaining a surface with reduced roughness by using a planarization process configured with a selectivity of the crystalline material to the insulator greater than one. In a preferred embodiment, the planarization process uses a composition including abrasive spherical silica, H_2O_2 and water. In a preferred embodiment, the area confined by the insulator is an opening in the insulator having an aspect ratio sufficient to trap defects using an ART technique.

15 Claims, 17 Drawing Sheets